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09/955,885	09/19/2001	Yasutoshi Hirano	2271/65888	9849

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EXAMINER	
TRAN, DENISE	

ART UNIT	PAPER NUMBER
2186	6

DATE MAILED: 04/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,885	HIRANO, YASUTOSHI	
	Examiner	Art Unit	
	Denise Tran	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The applicant's amendment filed 2/9/04 has been considered. Claims 1-14 are presented for examination.

2. The objection to the specification as failing to provide proper antecedent basis for the claimed subject matter is **withdrawn** due to the applicant's arguments filed 2/9/04.

3. The objections to the drawings under 37 CFR 1.83(a) is **withdrawn** due to the proposed drawing change to fig. 1, filed 2/9/04.

4. The objection to claim 8 is **withdrawn** due to the applicant's amendment filed 2/9/04.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pawate et al., U.S. Patent No. 5,638,530 (hereinafter Pawate) in view of Hudson et al., U.S. Patent No. 6,088,785 (hereinafter Hudson).

As per claim 1, Pawate shows the use of signal processing apparatus (e.g. figure 2) comprising:

a digital signal processor (e.g. element 100, figure 2) comprising an internal memory part storing a program to be executed (e.g. element 150, 160, figure 2);

an external memory part storing programs executable in the digital signal processor (e.g. col. 13, line 59 to col. 14, line 48) (it is an inherent feature that when the host downloads information to the shared memory of the DSP processor it is doing it from the host memory inside the PC (e.g. element 200, figure 1) because this allows the information to be stored and then used at a later time, such as downloading it);

a clock signal generating part generating a clock signal and outputting the clock signal to the digital signal processor (e.g. element 181, figure 2); and

a clock signal control part controlling outputting of the clock signal to the digital signal processor so that the programs stored in the external memory part can be forwarded to the internal memory part (e.g. col. 13, line 59 to col. 14, line 48 and figure 2, elements 110-140, 180).

Pawate does not specifically show the use of wherein the control of output of the clock signal is performed without requiring reinitialization of the digital signal processor. Hudson shows the use of wherein the control of output of a signal is performed without requiring reinitialization of the digital signal processor (e.g. col. 18, line 53 to col. 19, line 40; col. 14, lines 47-68). In addition, Hudson shows the use of placing the individual subsystems in low power mode and halt mode which permits the subsystem to operate at a lower frequency, utilizing the lower frequency clock (e.g. col. 14, lines 47-68). It

would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Hudson with Pawate because it would provide for dynamic loading of the DSP memory without having the subsystem to be reset, therefore, allowing for a reduction in memory size and increasing processing speed.

As per claim 2, Pawate shows the use of the clock signal control part forwards the programs read from said external memory part to the internal memory after stopping outputting the clock signal to the digital signal processor (e.g. col. 13, line 59 to col. 14, line 48).

As per claim 3, Pawate shows the use of the clock signal control part comprises a forward circuit part and a clock control part, the clock control part stops outputting the clock signal to the digital signal processor after the forward circuit part supplies the clock control part with a signal requesting that the clock control part stops outputting the clock signal to the digital signal processor so that the programs stored in the external memory part can be forwarded to the internal memory part (e.g. col. 13, line 59 to col. 14, line 58).

As per claim 4, Pawate shows the use of the clock control part restarts outputting the clock signal to the digital signal processor after the forward circuit part supplies the clock control part with a signal requesting that the clock control part outputs the clock signal to the digital signal processor when the programs stored in the external

memory part are completely forwarded to the internal memory part (e.g. col. 13, line 59 to col. 14, line 58).

As per claims 5 and 6, Pawate shows the use of the clock signal control part controls outputting of the clock signal to the digital signal processor in compliance with a request from the digital signal processor (e.g. col. 9, lines 1-15) and in compliance with a request from an outside of the signal processing apparatus (e.g. col. 14, lines 5-10).

As per claim 7, Pawate shows the use of the clock signal control part comprises a forward circuit for forwarding a desired part of the programs read from the external memory part to the internal memory (e.g. element 180, figure 2).

7. Claims 8-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima et al., JP01264034A (hereinafter Nakajima, in view of Pawate et al., U.S. Patent No. 5,638,530 (hereinafter Pawate) and further view of Hudson et al., U.S. Patent No. 6,088,785 (hereinafter Hudson).

As per claim 8, Nakajima shows the use of a modem for modulating / demodulating a communication data by using a signal processing apparatus (e.g. abstract) comprising:

A digital signal processor comprising an internal memory part storing a program to be executed (e.g. abstract and figure 1). Nakajima does not disclose an external

memory part storing programs executable in said digital signal processor; a clock signal generating a clock signal and outputting the clock signal to said digital signal processor to said digital signal processor; and a clock signal control part controlling outputting of said clock signal to said digital signal processor so that said programs stored in said external memory part can be forwarded to said internal memory part and wherein the control of output of the clock signal is performed without requiring reinitialization of the digital signal processor.

Pawate shows the use of a digital signal processor (e.g. element 100, figure 2) comprising an internal memory part storing a program to be executed (e.g. element 150, 160, figure 2);

an external memory part storing programs executable in the digital signal processor (e.g. col. 13, line 59 to col. 14, line 48) (it is an inherent feature that when the host downloads information to the shared memory of the DSP processor it is doing it from the host memory inside the PC (e.g. element 200, figure 1) because this allows the information to be stored and then used at a later time, such as downloading it);

a clock signal generating part generating a clock signal and outputting the clock signal to the digital signal processor (e.g. element 181, figure 2); and

a clock signal control part controlling outputting of the clock signal to the digital signal processor so that the programs stored in the external memory part can be forwarded to the internal memory part (e.g. col. 13, line 59 to col. 14, line 48 and figure 2, elements 110-140, 180).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Pawate with Nakajima because it would provide for the re-configuration of the modem with additional programs and allowing the host to directly access the memory without arbitration. Hudson shows the use of wherein the control of output of a signal is performed without requiring reinitialization of the digital signal processor (e.g. col. 18, line 53 to col. 19, line 40 and col. 14, lines 47-68). In addition, Hudson shows the use of placing the individual subsystems in low power mode and halt mode which permits the subsystem to operate at a lower frequency, utilizing the lower frequency clock (e.g. col. 14, lines 47-68). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Hudson with Pawate and Nakajima because it would provide for dynamic loading of the DSP memory without having the subsystem to be reset, therefore, allowing for a reduction in memory size and increasing processing speed.

As per claim 9, Nakajima does not specifically show the limitations of claim 9. Pawate teaches the use of the clock signal control part forwards the programs read from said external memory part to the internal memory after stopping outputting the clock signal to the digital signal processor (e.g. col. 13, line 59 to col. 14, line 48).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Pawate with Nakajima because it would provide for the re-configuration of the modem with additional programs and allowing the host to directly access the memory without arbitration.

As per claim 10, Nakajima does not specifically show the limitations of claim 10. Pawate teaches the use of the clock signal control part comprises a forward circuit part and a clock control part, the clock control part stops outputting the clock signal to the digital signal processor after the forward circuit part supplies the clock control part with a signal requesting that the clock control part stops outputting the clock signal to the digital signal processor so that the programs stored in the external memory part can be forwarded to the internal memory part (e.g. col. 13, line 59 to col. 14, line 58). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Pawate with Nakajima because it would provide for the re-configuration of the modem with additional programs and allowing the host to directly access the memory without arbitration.

As per claim 11, Nakajima does not specifically show the limitations of claim 11. Pawate teaches the use of the clock control part restarts outputting the clock signal to the digital signal processor after the forward circuit part supplies the clock control part with a signal requesting that the clock control part outputs the clock signal to the digital signal processor when the programs stored in the external memory part are completely forwarded to the internal memory part (e.g. col. 13, line 59 to col. 14, line 58). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Pawate with Nakajima because it would provide for the re-configuration of the modem with additional programs and allowing the host to directly access the memory without arbitration.

As per claims 12 and 13, Nakajima does not specifically show the limitations of claims 12 and 13. Pawate teaches the use of the clock signal control part controls outputting of the clock signal to the digital signal processor in compliance with a request from the digital signal processor (e.g. col. 9, lines 1-15) and in compliance with a request from an outside of the signal processing apparatus (e.g. col. 14, lines 5-10). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Pawate with Nakajima because it would provide for the re-configuration of the modem with additional programs and allowing the host to directly access the memory without arbitration.

As per claim 14, Nakajima does not specifically show the limitations of claim 14. Pawate teaches the use of the clock signal control part comprises a forward circuit for forwarding a desired part of the programs read from the external memory part to the internal memory (e.g. element 180, figure 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Pawate with Nakajima because it would provide for the re-configuration of the modem with additional programs and allowing the host to directly access the memory without arbitration.

8. Applicant's arguments filed 02/09/04 have been considered but are not persuasive.

9. In the remarks, Applicants argued in substance that (1) the cited art, Pawate fails to show a signal processing apparatus which includes a digital signal processor, an external memory part, a clock signal generating a clock signal, and a clock signal control part, wherein the digital signal processor includes an internal memory part which stores a program to be executed, the clock signal control part controls output of the clock signal to the digital signal processor so that one or more of the programs stored in the external memory part can be forwarded to the internal memory part, and the control of output of the clock signal is performed without requiring reinitialization of the digital signal processor as provided by independent claim 1 as amended.

The examiner disagrees with the applicant's argument (1) because as stated in the above rejection to claim 1, the combination of Pawate and Hudson shows all the claimed limitations. In particular, Pawate shows the use of signal processing apparatus (e.g. figure 2) comprising:

a digital signal processor (e.g. element 100, figure 2) comprising an internal memory part storing a program to be executed (e.g. element 150, 160, figure 2);

an external memory part storing programs executable in the digital signal processor (e.g. col. 13, line 59 to col. 14, line 48) (it is an inherent feature that when the host downloads information to the shared memory of the DSP processor it is doing it from the host memory inside the PC (e.g. element 200, figure 1) because this allows the information to be stored and then used at a later time, such as downloading it);

a clock signal generating part generating a clock signal and outputting the clock signal to the digital signal processor (e.g. element 181, figure 2); and

a clock signal control part controlling outputting of the clock signal to the digital signal processor so that the programs stored in the external memory part can be forwarded to the internal memory part (e.g. col. 13, line 59 to col. 14, line 48 and figure 2, elements 110-140, 180).

Pawate does not specifically show the use of wherein the control of output of the clock signal is performed without requiring reinitialization of the digital signal processor. Hudson shows the use of wherein the control of output of a signal is performed without requiring reinitialization of the digital signal processor (e.g. col. 18, line 53 to col. 19, line 40; col. 14, lines 47-68). In addition, Hudson shows the use of placing the individual subsystems in low power mode and halt mode which permits the subsystem to operate at a lower frequency, utilizing the lower frequency clock (e.g. col. 14, lines 47-68). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Hudson with Pawate because it would provide for dynamic loading of the DSP memory without having the subsystem to be reset, therefore, allowing for a reduction in memory size and increasing processing speed.

Therefore, the combination of references shows all the claimed limitations and render the claimed invention unpatentable.

10. In the remarks, Applicants argued in substance that (2) claim 8 is patentable distinct from the cited art for at least similar reasons.

The examiner disagrees with the applicant's argument (2) because as stated in the above rejection to claim 8, the combination of Nakajima, Pawate and Hudson shows

all the claimed limitations. In particular, Nakajima shows the use of a modem for modulating / demodulating a communication data by using a signal processing apparatus (e.g. abstract) comprising:

A digital signal processor comprising an internal memory part storing a program to be executed (e.g. abstract and figure 1). Nakajima does not disclose an external memory part storing programs executable in said digital signal processor; a clock signal generating a clock signal and outputting the clock signal to said digital signal processor to said digital signal processor; and a clock signal control part controlling outputting of said clock signal to said digital signal processor so that said programs stored in said external memory part can be forwarded to said internal memory part and wherein the control of output of the clock signal is performed without requiring reinitialization of the digital signal processor.

Pawate shows the use of a digital signal processor (e.g. element 100, figure 2) comprising an internal memory part storing a program to be executed (e.g. element 150, 160, figure 2);

an external memory part storing programs executable in the digital signal processor (e.g. col. 13, line 59 to col. 14, line 48) (it is an inherent feature that when the host downloads information to the shared memory of the DSP processor it is doing it from the host memory inside the PC (e.g. element 200, figure 1) because this allows the information to be stored and then used at a later time, such as downloading it);

a clock signal generating part generating a clock signal and outputting the clock signal to the digital signal processor (e.g. element 181, figure 2); and

a clock signal control part controlling outputting of the clock signal to the digital signal processor so that the programs stored in the external memory part can be forwarded to the internal memory part (e.g. col. 13, line 59 to col. 14, line 48 and figure 2, elements 110-140, 180).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Pawate with Nakajima because it would provide for the re-configuration of the modem with additional programs and allowing the host to directly access the memory without arbitration. Hudson shows the use of wherein the control of output of a signal is performed without requiring reinitialization of the digital signal processor (e.g. col. 18, line 53 to col. 19, line 40 and col. 14, lines 47-68). In addition, Hudson shows the use of placing the individual subsystems in low power mode and halt mode which permits the subsystem to operate at a lower frequency, utilizing the lower frequency clock (e.g. col. 14, lines 47-68). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Hudson with Pawate and Nakajima because it would provide for dynamic loading of the DSP memory without having the subsystem to be reset, therefore, allowing for a reduction in memory size and increasing processing speed.

Therefore the combination of references shows all the claimed limitations and render the claimed invention unpatentable.

11. The other Applicant's arguments with respect to claims 1 and 8 have been considered but are moot in view of the new ground(s) of rejection necessitated by applicant's amendment.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday, Thursday and an alternated Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for central Official communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

D.T.
April 18, 2004